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10/706,576	11/12/2003	Tongbi Jiang	2269-4886.1US (01-0201.01	6662

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EXAMINER	
DOLAN, JENNIFER M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 06/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/706,576	JIANG ET AL.	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *4/13/04 (pre-Amdt)*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/12/03;2/5/04;*. 2/7/05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 13-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 13 depends upon claim 1, which states that at least one first-level semiconductor device is provided within the receptacle and having a backside substantially coplanar with the lower surface of the substrate. Claim 13 adds the limitation that another first-level semiconductor device is provided within the receptacle and having a backside facing the backside of the first device. These claims are mutually contradictory, since either the 'another first level' device would end up positioned completely below the lower surface of the substrate, and thus not in the receptacle and not really a first-level device (but rather a third level device), or the 'first level' device does not have a backside substantially coplanar with the lower surface of the interposer substrate. Hence, it is unclear as to what the applicant is claiming in claims 13-17.

For the purposes of examination, it is assumed that both the 'first level' and the 'another first level' devices are provided back to back in the receptacle, but the 'first level' device does

not have a backside substantially coplanar with the lower surface of the substrate (similar to the embodiment of figure 12).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 5-8, and 18-21 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,949,135 to Washida et al. (cited by applicant).

Regarding claim 1, Washida discloses a method for assembling a multi-die package, comprising: providing an interposer (701, 801) with a substantially planar substrate (figures 1, 2) and a receptacle formed substantially through the substrate (opening 701a, 801a), the substrate having an upper surface (upper surface of 701 in figure 1) and a lower surface (bottom surface of 701 in figure 1), the upper surface having conductors (706,806) thereon; positioning at least one first-level device (760) within the receptacle, a backside of the device being substantially coplanar with the lower surface of the substrate (figure 1); an interstitial space remaining at least between peripheral edges of the device and the substrate (figure 1); positioning a second level device (750) above the upper surface of the substrate (figure 1); electrically connecting the first-

level device to the conductors on the substrate and to the second-level device by first level conductive members (763; die 760 is connected to second die 750 and mounting board lands through solder-bump connections 763 to 753 and 707); and electrically connecting the second level device to the conductors on the upper surface of the substrate through second level conductive members (707).

Regarding claims 5 and 6, Washida discloses forming intermediate conductive elements (753, 707) between the bond pads of the first/second level device and the conductors of the interposer (figure 1).

Regarding claim 7, Washida discloses positioning the second level device over the interposer (column 4, line 65 – column 5, line 20).

Regarding claim 8, Washida discloses securing the first and second devices to one another before positioning the second level device (column 4, line 65 – column 5, line 10).

Regarding claim 18, Washida discloses providing an interposer (701) with a substantially planar substrate (figure 1) and a receptacle (701a) formed through the substrate; positioning a first semiconductor device (760) over a first (lower; figure 1) surface of the interposer, at least one bond pad (763) being exposed to the receptacle (figure 1); positioning a second device (750) over a second surface (top in figure 1) of the interposer, at least one bond pad (753) of the second device being exposed to the receptacle (figure 1); and electrically connecting the bond pads through the receptacle (figure 1).

Regarding claim 19, Washida discloses securing a conductive structure (either 707 or 706) to the bond pads of the second device (figure 1).

Regarding claim 20, Washida discloses that the securing of conductive elements (707) is effected before positioning (column 4, lines 50-65).

Regarding claim 21, Washida discloses that the securing of conductive elements (706) to the structure is effected after positioning (column 5, lines 1-20).

5. Claims 1-6 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,365,963 to Shimada (cited by applicant).

Regarding claim 1, Shimada discloses a method for assembling a multi-die package, comprising: providing an interposer (101) with a substantially planar substrate (figures 3, 4a-4d) and a receptacle (see figure 4a) formed substantially through the substrate, the substrate having an upper and lower surface (figure 4a), the upper surface having conductors thereon (103, 105, 106); positioning at least one first level device (11) within the receptacle (figures 4a-4c), the backside of the device being substantially coplanar with the lower surface of the substrate (figure 4c), an interstitial space remaining between the peripheral edges of the device and the substrate (figure 4c); positioning a second level device (12) above the upper surface of the substrate (figure 4d); electrically connecting the first level device to the conductors on the upper surface of the substrate and to the second device (through vias 104; see figures 4a-4d) by first level conductive members (by 21, 111, 104); and electrically connecting the second level device to the conductors on the upper surface by second level conductive members (22).

Regarding claims 2-4, Shimada discloses introducing a quantity of encapsulant material (107) to fill a portion of the interstitial space after electrically connecting the first-level device

(column 3, lines 40-55; encapsulant 107 deposited after both chips are connected); and introducing encapsulant between the first and second level devices (figure 4d).

Regarding claims 5 and 6, Shimada discloses positioning intermediate conductive elements between bond pads of the first-level device and interposer conductors (intermediate elements include 21, 111, 104), and between the bond pads of the second level device and the interposer conductors (intermediate elements include 22).

6. Claims 1-6 and 9-12 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,452,278 to DiCaprio et al. (cited by applicant).

Regarding claim 1, DiCaprio discloses a method for assembling a multi-die package, comprising: providing an interposer (14) having a substantially planar substrate (figures 3, 4) and a receptacle formed substantially through the substrate (see figures 6a-6c; column 2, lines 23-27), the substrate having upper and lower surfaces, wherein the upper surface has conductors thereon (16; figures 1-4); positioning at least one first level device (12) within the receptacle (figures 6a-6c; column 2, lines 23-28), a backside of the first level device being substantially coplanar with the lower surface of the substrate (figures 1-4), an interstitial space remaining between the peripheral edges of the device and the receptacle (figures 1-4; 6a-6c); positioning a second level device (42, 50, or 58) above the upper surface of the substrate (figures 2-4; second level device is 'above' the substrate); and electrically connecting the first level device to both the conductors on the substrate and to the second level device (figures 2-4; column 3, lines 15-25) and from second level devices to the conductors on the substrate by first and second level conductive members (24).

Regarding claims 2 and 3, DiCaprio discloses introducing encapsulant to fill at least a portion of the interstitial space (column 2, lines 14-24; figures 1-4), where the encapsulation occurs after forming the electrical connections (see figures 6c-6d; wirebonding must inherently occur before encapsulation).

Regarding claim 4, DiCaprio discloses introducing epoxy, which is an encapsulant-type material, between the first and second level devices (column 3, lines 30-35).

Regarding claims 5 and 6, DiCaprio discloses forming intermediate conductive elements (wirebonds 24) between the bond pads of the first and second level devices and the conductors of the interposer (figures 3 and 4).

Regarding claims 9 and 10, DiCaprio discloses providing a multi-interposer substrate (figure 7), which is singulated into individual assemblies (column 2, lines 20-23; column 4, lines 1-10).

Regarding claims 11 and 12, DiCaprio discloses adhering a film (70) to the lower surface of the substrate to cover a portion of the receptacle (column 4, lines 10-20) prior to the positioning of the first device therein (figures 6a-6b), and removing the adhered film from the lower surface following curing of the encapsulant in the receptacle (column 4, lines 20-30; figures 6d-6f).

7. Claims 18, 19, 21, and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,441,495 to Oka et al.

Regarding claim 18, Oka discloses providing an interposer with a substantially planar substrate (1a; figure 17, 18, 20, 23) and a receptacle formed substantially through the substrate

(12a); positioning a first device (2c) over a first surface of the interposer, at least one bond pad (23, 24) being exposed to the receptacle (figure 17); positioning a second device (2d) over a second surface of the interposer, at least one bond pad (22a) being exposed to the receptacle (figure 17); and electrically connecting the bond pads through the receptacle (figure 17; column 13, lines 15-55).

Regarding claims 19 and 21, Oka discloses that conductive structures 22a and 23 are secured to the bond pad of the opposite chip after positioning (column 13, lines 15-55).

Regarding claim 22, Oka discloses that the first device comprises a portion of a redistribution circuit (see column 13, lines 55-67; figures 17-18).

8. Claims 1, 7, and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,791,195 to Urushima et al.

Regarding claim 1, Urushima discloses a method for assembling a multi-die package, comprising: providing an interposer (48) having a substantially planar substrate (figure 11a) and a receptacle (51) formed substantially through the substrate (figure 11a), the substrate having upper and lower surfaces with conductors (35) on the upper surface (figure 11a); positioning at least one first-level device (3d) within the receptacle, where the backside is substantially coplanar with the lower surface of the substrate (figure 11c), an interstitial space remaining between peripheral edges of the device and substrate (figure 11a; a portion of 51 remains between device 3d and interposer 48); positioning a second level device (3c) above the upper surface of the substrate (figure 11a); electrically connecting the first level device to a conductor on the substrate (device 3d must be connected to interposer through traces on second level

devices, or it would not be able to be powered by the wiring board or communicate with the wiring board), connecting the first device to the second device (through 21); and electrically connecting the second device to the conductors on the substrate (through outer bumps 21; see figure 11a).

Regarding claim 7, Urushima discloses positioning the second level device in a flip-chip arrangement over the first level device; and positioning the second level device over the interposer (figure 11a).

Regarding claim 8, Urushima discloses securing the first and second level devices to one another before positioning the second device (figure 11b; column 20, lines 10-30).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Urushima in view of U.S. Patent Publication No. 2002/0047214 to Morinaga et al.

Urushima fails to disclose another first level device within the receptacle, where the first-level devices are back-to-back, where the 'another' first level device has bond pads connected to conductors on the lower surface of the interposer.

Morinaga discloses that two first level chips (6a and 6b) may be stacked back-to-back in a receptacle in the interposer (figure 5), where the 'another' first level chip is electrically connected to conductors (43) on the lower side of the substrate (figure 5).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the structure of Urushima, such that in place of the single chip in the receptacle, two first-level back-to-back chips are disposed in the receptacle, each chip being electrically connected to the nearest surface of the interposer, as suggested by Morinaga. The rationale is as follows: A person having ordinary skill in the art would have been motivated to dispose both chips in the receptacle, because doing so allows multiple same-sized chips to be packed in a small area, such that a reduced profile is achieved, and such that bonding wires connecting the chips to the interposer do not interfere with each other (see Morinaga, figure 5; paragraphs 0030-0034; 0044).

11. Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Urushima in view of Morinaga, as applied to claim 13 above, and further in view of U.S. Patent No. 6,388,333 to Taniguchi et al.

Urushima fails to teach a third-level device over the lower surface of the substrate.

Taniguchi discloses that interposers may be double-sided, such that devices are disposed in a substantially similar manner over both the top and bottom surfaces of the interposer (see figures 19, 33; column 14, lines 20-55), where the devices disposed on the bottom surface of the interposer are connected to the conductors on the lower surface of the interposer and where chips

on both sides of the interposer are electrically connected to each other (figure 19; column 14, lines 20-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the structure of Urushima as modified by Morinaga, such that the interposer is double-sided, with similar device structures attached to each side (i.e., a third device analogous to the second level device formed below the interposer, where the third device and 'another' first level device are interconnected, analogous to the connections between the first level device and second level device, and where the third level device is connected to the lower side of the interposer, analogous with the second level device being connected to the upper side of the interposer), as suggested by Taniguchi. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use a double-sided interposer, with 'mirrored' device structures on each side, because Taniguchi shows that such a stacking minimizes the total device height of the structure per chip on the interposer (Taniguchi, compare figure 18 with figure 19 or the bottom embodiment in figure 33 with any of the other embodiments), minimizes the length and mutual interference of wirebonds (Taniguchi, compare figure 18 with figure 19), and minimizes the required number of stacked interposers per chip in the module (Taniguchi, figure 33).

12. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over DiCaprio et al. in view of Morinaga et al.

DiCaprio fails to disclose another first level device within the receptacle, where the first-level devices are back-to-back, where the 'another' first level device has bond pads connected to conductors on the lower surface of the interposer.

Morinaga discloses that two first level chips (6a and 6b) may be stacked back-to-back in a receptacle in the interposer (figure 5), where the 'another' first level chip is electrically connected to conductors (43) on the lower side of the substrate (figure 5).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the structure of DiCaprio such that in place of the single chip in the receptacle, two first-level back-to-back chips are disposed in the receptacle, each chip being electrically connected to the nearest surface of the interposer, as suggested by Morinaga. The rationale is as follows: A person having ordinary skill in the art would have been motivated to dispose two chips in the receptacle, because doing so allows multiple same-sized chips to be packed in a small area, such that a reduced profile is achieved, and such that bonding wires connecting the chips to the interposer do not interfere with each other (see Morinaga, figure 5; paragraphs 0030-0034; 0044), and furthermore, the combination of DiCaprio and Morinaga would enable the connection of 3 chips on the module without significantly increasing the height profile of the structure (Morinaga, figure 5; DiCaprio, figures 3 and 4).

13. Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over DiCaprio et al. in view of Morinaga, as applied to claim 13 above, and further in view of U.S. Patent No. 6,388,333 to Taniguchi et al.

DiCaprio fails to teach a third-level device over the lower surface of the substrate.

Taniguchi discloses that interposers may be double-sided, such that devices are disposed in a substantially similar manner over both the top and bottom surfaces of the interposer (see figures 19, 33; column 14, lines 20-55), where the devices disposed on the bottom surface of the interposer are connected to the conductors on the lower surface of the interposer and where chips on both sides of the interposer are electrically connected to each other (figure 19; column 14, lines 20-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the structure of DiCaprio as modified by Morinaga, such that the interposer is double-sided, with similar device structures attached to each side (i.e., a third device analogous to the second level device formed below the interposer, where the third device and 'another' first level device are interconnected, analogous to the connections between the first level device and second level device, and where the third level device is connected to the lower side of the interposer, analogous with the second level device being connected to the upper side of the interposer), as suggested by Taniguchi. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use a double-sided interposer, with 'mirrored' device structures on each side, because Taniguchi shows that such a stacking minimizes the total device height of the structure per number of chips held (Taniguchi, compare figure 18 with figure 19 or the bottom embodiment in figure 33 with any of the other embodiments), minimizes the length and mutual interference of wirebonds (Taniguchi, compare figure 18 with figure 19), and minimizes the required number of stacked interposers per chip in the module (Taniguchi, figure 33).

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,693,362 to Seyama et al.,

U.S. Patent Publication No. 2003/0085463 to Gerber et al., and

U.S. Patent Publication No. 2002/0127770 to Vaiyapuri disclose alternate arrangements for interposers with first-level dice provided in a receptacle in an interposer, and second level device provided on the top or bottom surface of the interposer.

U.S. Patent Publication No. 2003/0025199 to Wu et al. discloses multiple dice stacked in a receptacle of an interposer.

U.S. Patent No. 6,343,019 to Jiang et al. discloses back-to-back dice stacked in a receptacle of an interposer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd

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